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Confirmation No. 9960

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant:	MUTH	Examiner:	Zaman, F.
Serial No.:	10/534,164	Group Art Unit:	2111
Filed:	May 5, 2005	Docket No.:	DE02 0252US
Title:	INTEGRATED CIRCUIT WITH LIN-PROTOCOL TRANSMISSION		

CERTIFICATH UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence and the papers, as described hereinabove, are being transmitted via facsimile-Formal Entry, to the attention of the Examiner at Commissioner for Patents, MAIL STOP APPEAL BRIEF, P.O. Box 1450, Alexandria, VA 22313-1450,
on August 14, 2007
By: Kelly J. Lebo
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Facsimile No.: 571 273-8300

APPEAL BRIEF

Mail Stop Appeal Brief-Patents
Commissioner For Patents
P.O. Box 1450
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Customer No.
65913

Dear Sir:

This Appeal Brief is submitted pursuant to 37 C.F.R. §41.37, in support of the Notice of Appeal filed June 14, 2007 and in response to the rejections of claims 1-6 as set forth in the Final Office Action dated March 13, 2007, and in further response to the Advisory Action dated May 7, 2007.

Please charge Deposit Account number 50-0996 (NXPS.206PA) $500.00 for filing this brief in support of an appeal as set forth in 37 C.F.R. §1.17(c). If necessary, authority is given to charge/credit Deposit Account 50-0996 (NXPS.206PA) additional fees/overages in support of this filing.

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I. Real Party In Interest

The real party in interest is NXP Semiconductors. The application is presently assigned of record, at reel/frame nos. 017461/0075 to Koninklijke Philips Electronics, N.V., headquartered in Eindhoven, the Netherlands. We have been authorized by both the assignee of record and NXP Semiconductors to convey herein that the entire right, title and interest of the instant patent application have been transferred to NXP Semiconductors.

II. Related Appeals and Interferences

While Appellant is aware of other pending applications owned by the above-identified Assignee, Appellant is unaware of any related appeals, interferences or judicial proceedings that would have a bearing on the Board's decision in the instant appeal.

III. Status of Claims

Claims 1-6 stand rejected. Accordingly, claims 1-6 are presented for appeal. A complete listing of the claims under appeal is provided in an Appendix to this Brief.

IV. Status of Amendments

No amendments have been filed subsequent to the Preliminary Amendment entered on May 5, 2005.

V. Summary of Claimed Subject Matter

Commensurate with independent claim 1, an example embodiment of the present invention is directed to an integrated circuit (*e.g.*, FIG. 1, element 1; paragraphs 22-25) having a system base chip that has basic functions for a transmitting and/or receiving system for a vehicle data bus (*e.g.*, paragraph 35), namely at least a system voltage supply (*e.g.*, FIG. 1, element 3; paragraph 26), a system reset (*e.g.*, FIG. 1, element RST; paragraph 27) and a monitoring function (*e.g.*, FIG. 1, element 2; paragraph 28). An interface circuit (*e.g.*, FIG. 1, element 4; paragraph 29), in a self-contained fashion, runs at least parts of a data bus protocol, and in particular the LIN (Local Interconnect Network) protocol, that performs detection of the bit-rate of received data, and that is capable of passing on at least one

received or transmitted byte (*e.g.*, paragraphs 29-33). A serial/parallel converter (*e.g.*, FIG. 1 element 5; paragraph 33) makes use in its conversion of the bit-rate detected by the interface circuit.

As required by 37 C.F.R. § 41.37(c)(1)(v), a concise explanation of the subject matter defined in the independent claims involved in the appeal is provided herein. Appellant notes that representative subject matter is identified for these claims; however, the abundance of supporting subject matter in the application prohibits identifying all textual and diagrammatic references to each claimed recitation. Appellant thus submits that other application subject matter, which supports the claims but is not specifically identified above, may be found elsewhere in the application. Appellant further notes that this summary does not provide an exhaustive or exclusive view of the present subject matter, and refers to the specification, including the appended claims and their legal equivalents, for additional example embodiments.

VI. Grounds of Rejection to be Reviewed Upon Appeal

1. Claims 1 and 6 stand rejected under 35 U.S.C. § 103(a) over Feuerstraeter *et al.* (U.S. Publ. 2003/0058894) "AAPA" (Applicant's Admitted Prior Art) and Ishikuri (U.S. 6,674,681).
2. Claims 2 and 3 stand rejected under 35 U.S.C. § 103(a) over Feuerstraeter, AAPA, and Ishikuri as applied to claim 1, and further in view of Bongiorno *et al.* (U.S. 6,292,045).
3. Claims 4 and 5 stand rejected under 35 U.S.C. § 103(a) over Feuerstraeter, AAPA and Ishikuri, and further in view of Werle (U.S. 5,778,002).

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VII. Argument

A. The Section 103(a) rejections of claims 1 and 6 over Feuerstraeter *et al.* (U.S. Publ. 2003/0058894) "AAPA" (Applicant's Admitted Prior Art) and Ishikuri (U.S. 6,674,681)

1) Claims 1 and 6: The rejections are improper because they lack any reason to combine, would defeat the purpose of the references, and they fail to teach each limitation.

a) There is no reason to combine the elements in the manner suggested by the Examiner.

The record shows that Examiner has improperly combined individual elements of the claimed invention without performing the necessary analysis under 35 U.S.C. § 103. As supported by a recent Supreme Court case, merely identifying elements in the prior art is not enough to show obviousness: "a patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art...inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known." KSR Int'l Co. v. Teleflex Inc., 127 S. Ct. 1727, 1741 (U.S. 2007).

In this instance, the Examiner's reason for combining the references (per the Final Office Action of March 13, 2007) is taken from the Feuerstraeter reference and is for the purpose of providing an interface such that "one or more devices may communicate with each other when otherwise the devices would not." See the Final Office Action of March 13, 2007. This reason relies upon the premise that the devices could not otherwise communicate. The record clearly shows that the devices of AAPA can communicate with each other. More particularly, the citation from the Feuerstraeter reference, when taken in context, deals with providing an interface for two different protocols (WAN and LAN) which were previously unable to communicate with each other. See Feuerstraeter *et al.* AAPA, as discussed in detail below, already incorporates such an interface. Thus, the Examiner has not shown any reason why one of skill in the art would find the asserted combination obvious.

Generally, the AAPA discusses the problems associated with two devices, which communicate using LIN protocol, being able to use a standard SCI/UART (Serial

Communication Interface/Universal Asynchronous Receiver Transmitter) interface to communicate with each other. *See, e.g.,* Appellant's Specification, Paragraph 0003. To enable communication between these devices, the AAPA requires a specially adapted interface and a specially adapted external microcontroller that performs the bit-rate detection. *See, e.g.,* Appellant's Specification, Paragraphs 0004 and 0030. The instant application includes claimed limitations that are directed to the elimination of the need for a specially adapted external microcontroller by enabling the interface circuit to perform the bit-rate detection thereby allowing the use of any available microcontroller. *See, e.g.,* Appellant's Specification, Paragraph 0013. In this regard, the AAPA already allows two devices to communicate with each other using LIN protocols and experiences no issues relative to this communication. Accordingly, absent Feuerstracter's teachings, the devices *would* communicate with each other and the Examiner's reason for combining the references is not present. As such, there is no motivation to modify the AAPA based upon Feuerstracter's teachings directed to enabling devices using different protocols to communicate with each other because the devices of the AAPA are already capable of communicating with each other. Accordingly, the Section 103(a) rejections of claims 1 and 6 are improper and must be reversed.

b) <u>The Examiner has relied upon improper hindsight reconstruction.</u>

The Examiner has improperly used the Appellant's invention as a template for the asserted combination of references. "It is impermissible, however, simply to engage in a hindsight reconstruction of the claimed invention, using the appellant's structure as a template and selecting elements from references to fill the gaps." *In re Gorman*, 933 F.2d 982, 987 (Fed. Cir. 1991). In this instance, The Examiner has used a shifting rationale for combining the references which relies on various quotations taken from the references without properly addressing the claimed invention as a whole. The Examiner's rationale for combining the references has not been viewed in the context of the asserted combination or in the context of the claimed invention as a whole. The Examiner's shifting rationale behind different attempts at combining the elements creates a strong inference that the Examiner has used Appellant's invention to select and combine the elements using improper hindsight

reconstruction. As no proper rationale remains for the Examiner's repeated attempts at combining the elements in various fashions and for various reasons, it appears that the underlying rationale was in fact improperly taken from Appellant's invention. More specifically, in the Office Action of November 15, 2006, the Examiner asserted a first combination of the elements in a manner that failed to view the invention as a whole and was inconsistent with the teachings of the cited references. See Appellant's Response of February 9, 2007. In the following Final Office Action of March 13, 2007, the Examiner presented a new combination that, while relying generally on the same references, was configured in a new manner and accompanied with yet another supposed rationale for combining the references. As the record shows and as discussed above, this rationale once again improperly ignored the invention as a whole. Appellant submits that the shifting explanations and combinations strongly imply that the Examiner has improperly used the Appellant's specification as the basis for the current combination of elements. Accordingly, the Section 103(a) rejections of claims 1 and 6 are improper and must be reversed.

c) The asserted combination of references would defeat the purpose of the primary reference.

Consistent with MPEP § 2143.01 and *In re Gordon*, 733 F.2d 900 (Fed. Cir. 1984), a § 103 obvious-type rejection cannot be maintained when the asserted modification undermines the purpose of the primary reference (a LIN protocol receiver as asserted here). The record shows that the asserted combination would not function properly in a LIN protocol environment. More specifically, the asserted combination would not be capable of receiving and transmitting information using the LIN protocol.

The Examiner is relying upon portions of the Feuerstraeter reference to teach a system base chip, an interface circuit or a serial/parallel converter. The Examiner asserts that these elements, allegedly in the Feuerstraeter reference, can be combined with the AAPA's LIN (Local Interconnect Network) protocols. However, for the Examiner's combination to function, the LAN and WAN-based circuits (i.e., TCP/IP Ethernet protocols) in the cited Feuerstraeter reference would need to function using a LIN protocol or otherwise correspond to the claimed limitations. Appellant notes that a receiver designed for TCP/IP WAN/LAN

protocols cannot be merely substituted into an environment that uses a LIN protocol. As such, after a careful review of the Feuerstraeter reference, Appellant cannot ascertain how the proposed combination would or could correspond to the claimed limitations; no portion of the Feuerstraeter reference mentions the LIN protocol or describes any aspect of the indicated system that could operate with protocols other than WAN or LAN protocols. Accordingly, the Section 103(a) rejections of claims 1 and 6 are improper and must be reversed.

d) The cited references fail to teach each limitation of the claimed invention.

In addition to the above lack of correspondence in the Feuerstraeter reference, the cited portions of the Ishikuri reference also do not correspond to the claim limitations directed to the system voltage supply and the system reset. The Examiner suggests adding a power on clear (POC) circuit and a system reset (POC circuit 1) from the Ishikuri reference to the AAPA and asserts that this addition teaches the claimed system voltage supply and system reset functions. The POC circuit 1 not only fails to correspond to the claimed power supply, it cannot act as such because its function is to work independently from such a power supply. Generally, POC circuits operate independently from a system power supply, and provide functionality that is independent from the same (*see, e.g.*, the Abstract and Background of the Ishikuri reference). For example, as described at Col. 5:52-55 in Ishikuri, the POC circuit 1 includes a detection voltage source 5 that does not correspond to a system voltage supply, which is separate from the POC circuit 1 (*e.g.*, the POC circuit 1 conducts a system reset when the system power supply drops below a certain voltage level as described at Col. 5:57-60). The Examiner in the Response to Argument Section of the Final Office Action of March 13, 2007 (*see, e.g.*, Page 8:2-9) appears to be confusing Ishikuri's POC circuit 1 with a circuit that receives a voltage, converts that voltage into a supply voltage and then provides the supply voltage to other components. Ishikuri's POC circuit 1 receives a power supply voltage and provides a POC output signal to AND gate 12; the POC circuit is not providing any power to the other parts of integrated circuit 100, it simply monitors the power supply voltage and provides a reset signal when the supply voltage drops below a

certain level. *See, e.g.*, Figure 1 and Col. 5:43-60. Accordingly, Ishikuri's POC circuit 1 does not correspond to the claimed system voltage supply and the Section 103(a) rejections of claims 1 and 6 are improper and must be reversed.

B. The Section 103(a) rejections of claims 2-5.

1. The rejections are improper because they lack any reason to combine, would defeat the purpose of the references, and they fail to teach each limitation.

a) Each of claims 2-5 depend from independent claim 1.

The Section 103(a) rejections of all of the dependent claims 2-5 (which depend from claim 1), must also be reversed in view of the above discussion regarding the independent claim rejections. That is, where an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. *See, e.g., In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988). In this regard, further discussion of claims 2-5 is unnecessary and the rejections must be reversed in view of the above discussion.

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VIII. Conclusion

In view of the above, Appellant submits that the rejection of claims 1-6 are improper. Appellant therefore requests reversal of the rejections as applied to the appealed claims and allowance of the entire application.

Authority to charge the undersigned's deposit account was provided on the first page of this brief.

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APPENDIX OF CLAIMS INVOLVED IN THE APPEAL
(S/N 10/534,164)

1. (Previously Presented) An integrated circuit having a system base chip that has basic functions for a transmitting and/or receiving system for a vehicle data bus, namely at least a system voltage supply, a system reset and a monitoring function,

an interface circuit that, in a self-contained fashion, runs at least parts of a data bus protocol, and in particular the LIN (Local Interconnect Network) protocol, that performs detection of the bit-rate of received data, and that is capable of passing on at least one received or transmitted byte,

a serial/parallel converter that makes use in its conversion of the bit-rate detected by the interface circuit.

2. (Previously Presented) An integrated circuit as claimed in claim 1, characterized in that there is provided in the integrated circuit an R/C oscillator that acts as a clock-signal source and as a timebase for the bit-rate detection.

3. (Previously Presented) An integrated circuit as claimed in claim 2, characterized in that the clock signal generated by the R/C oscillator may also be provided to circuits outside the integrated circuit, and in particular to a microprocessor.

4. (Previously Presented) An integrated circuit as claimed in claim 1, characterized in that the interface circuit may also pass on complete messages.

5. (Previously Presented) An integrated circuit as claimed in claim 1, characterized in that the interface circuit performs buffer-storage of data received or to be transmitted.

6. (Previously Presented) An integrated circuit as claimed in claim 1, characterized in that the serial/parallel converter converts serial data conforming to the SCI/UART (Serial Communication Interface/Universal Asynchronous Receiver Transmitter) interface standard into parallel data, or vice versa.

APPENDIX OF EVIDENCE

Appellant is unaware of any evidence submitted in this application pursuant to 37 C.F.R. §§ 1.130, 1.131, and 1.132.

APPENDIX OF RELATED PROCEEDINGS

As stated in Section II above, Appellant is unaware of any related appeals, interferences or judicial proceedings.